

This cross-sectional view shows the device structure along line X1-X2. It features a substrate 110 with a top layer 111. A central layer 120 is formed on the substrate, with a top layer 121 and a bottom layer 122. A layer 130 is formed on top of layer 120, with a top layer 131 and a bottom layer 132. A layer 140 is formed on top of layer 130, with a top layer 141 and a bottom layer 142. A layer 150 is formed on top of layer 140, with a top layer 150a and a bottom layer 150b. The layers are separated by interfaces 113, 113a, 132a, 143, 142, 150a, 122, 123a, and 123. The device is shown in a cross-section along line X1-X2.

[illegible]

FIG. 6

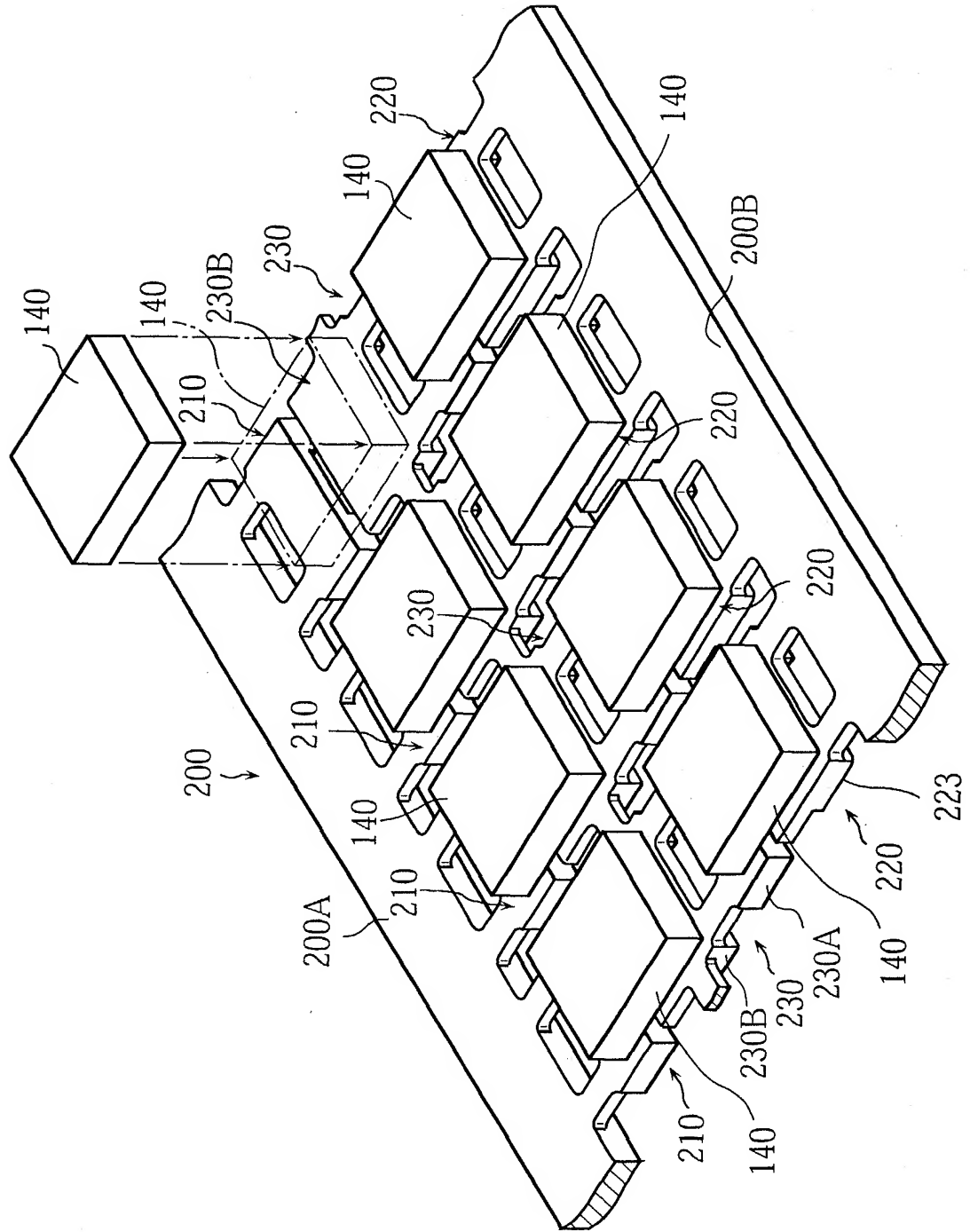


FIG. 7

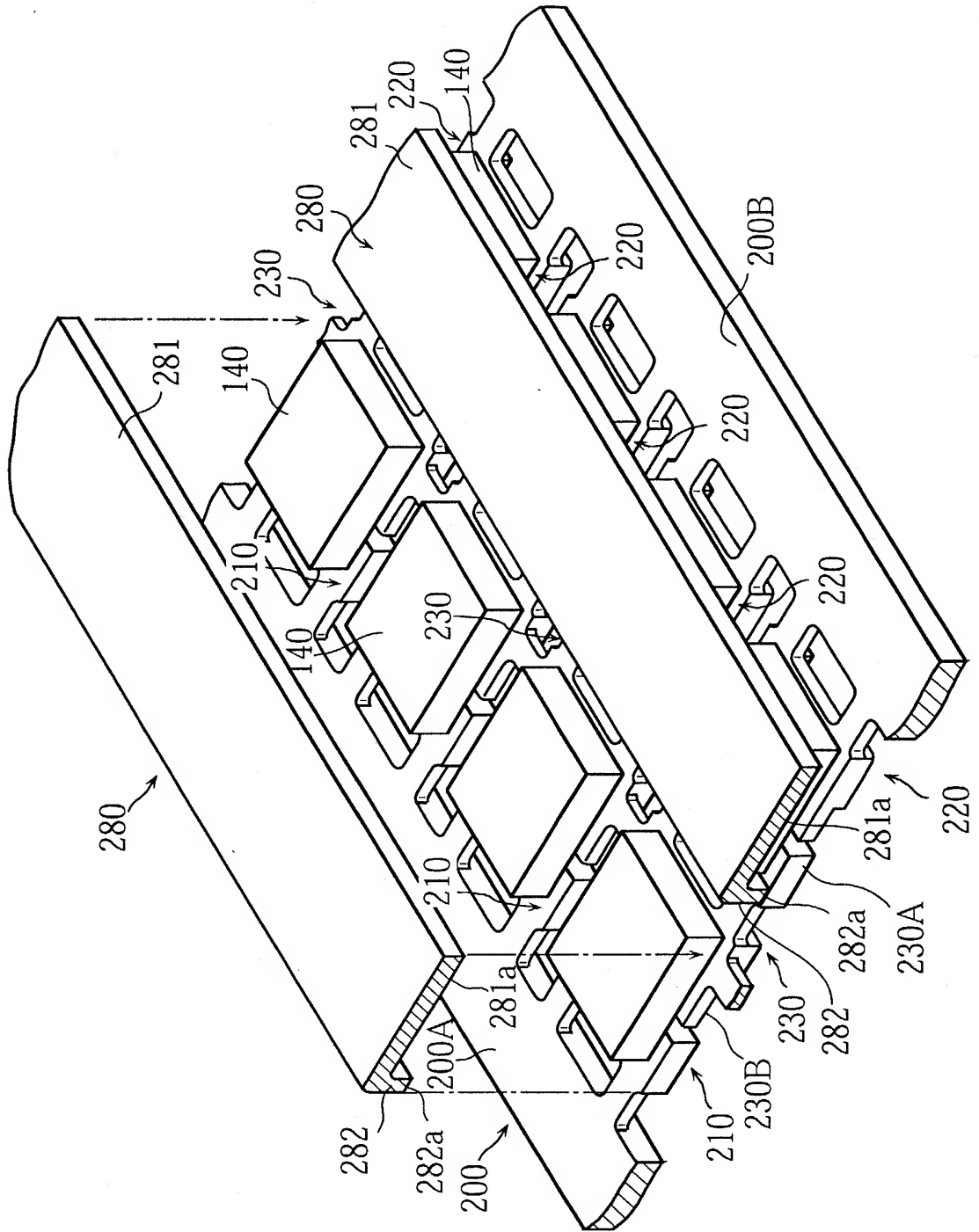


FIG. 8

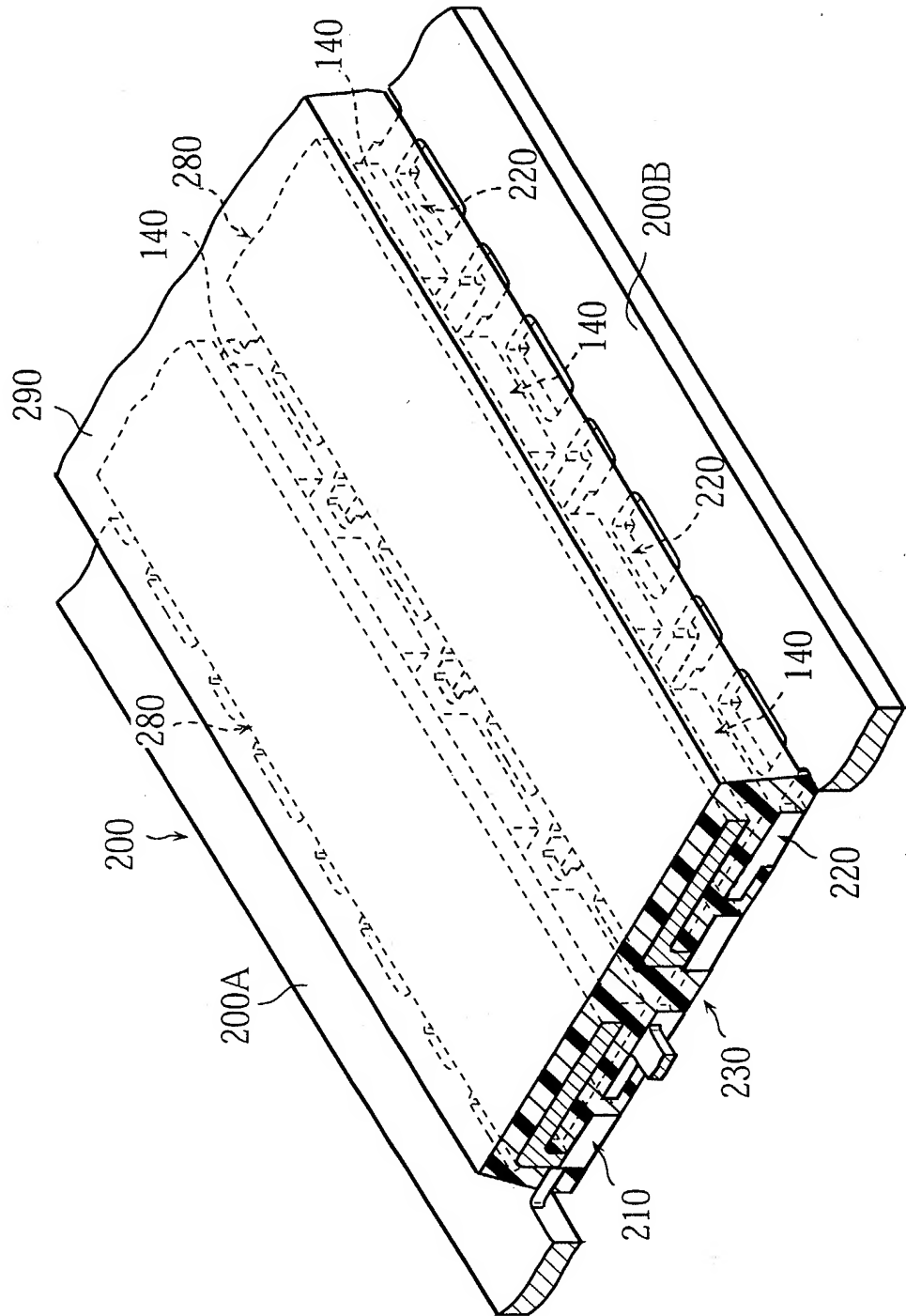


FIG. 9

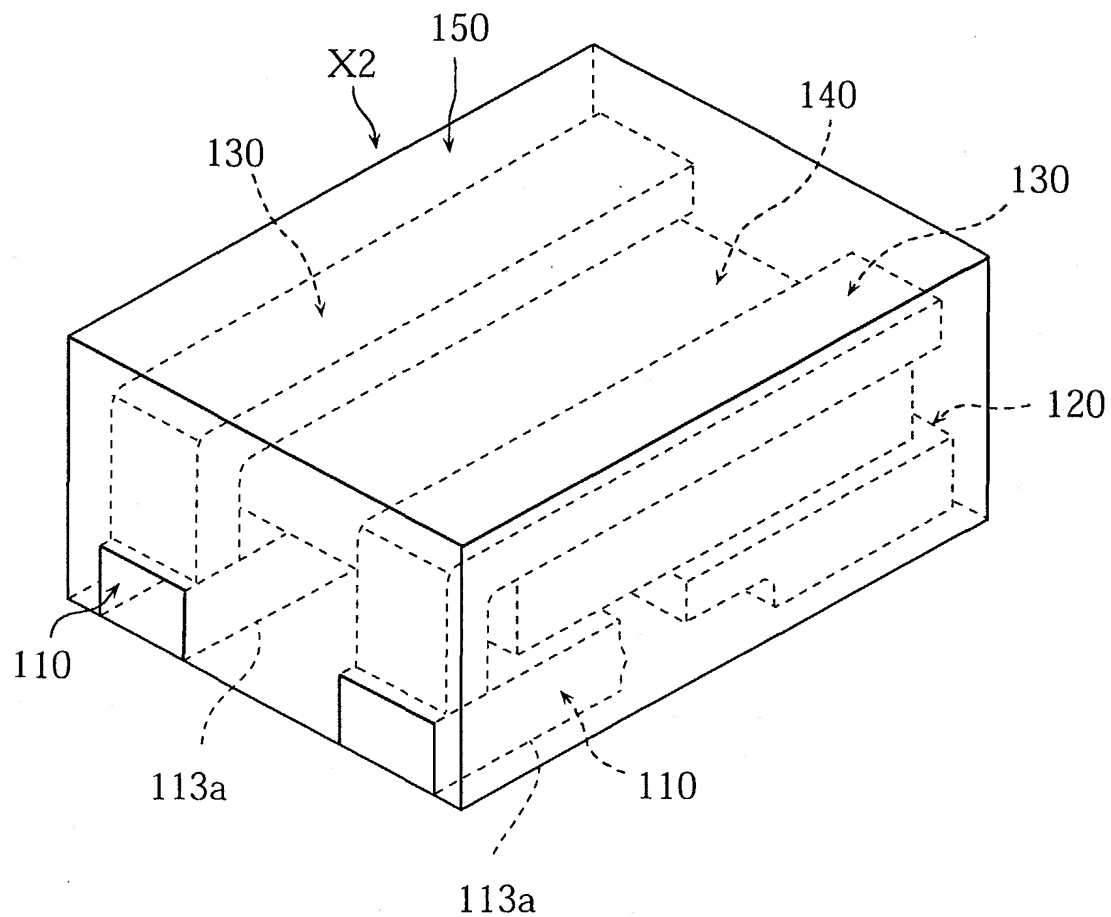


FIG. 10

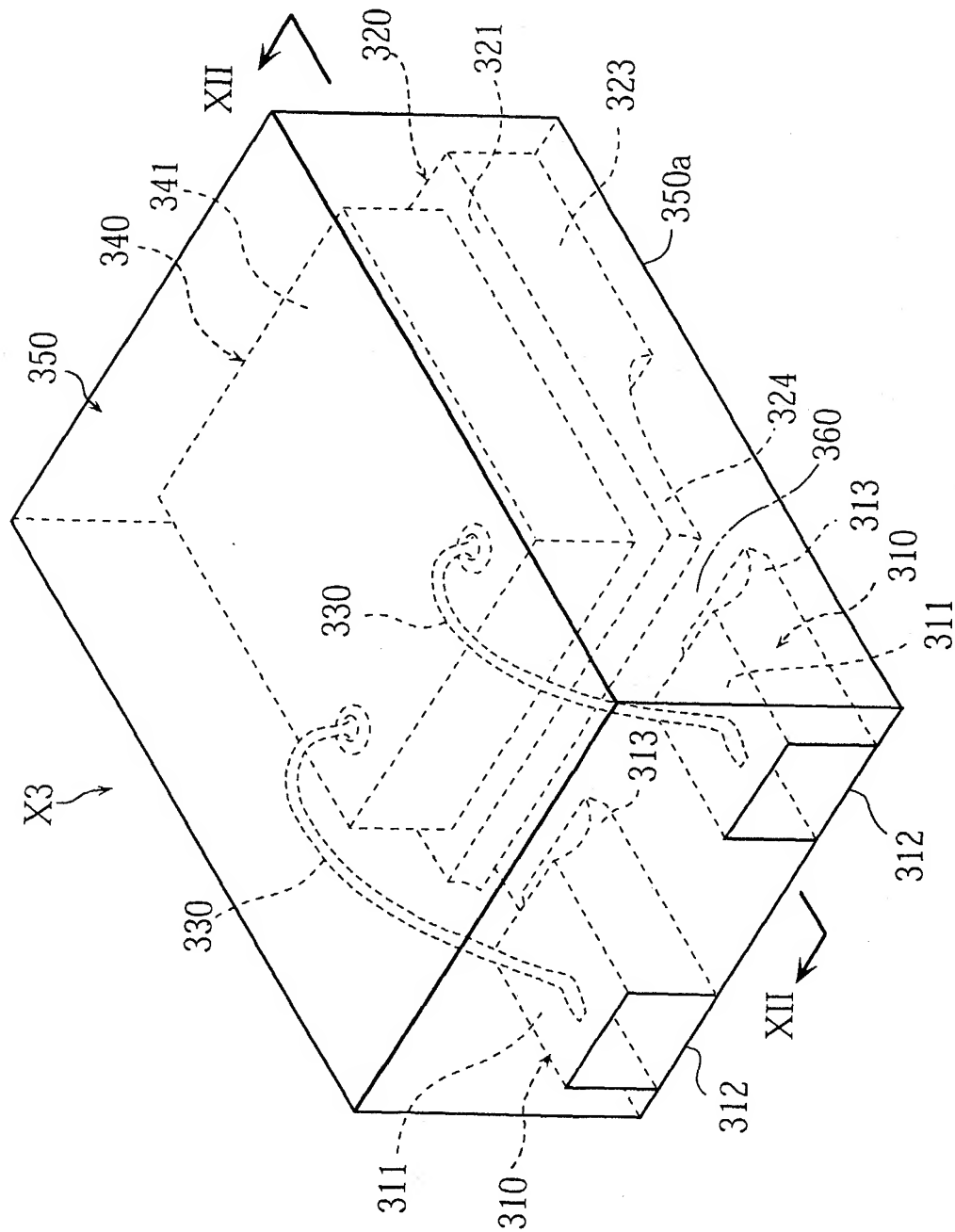


FIG. 12

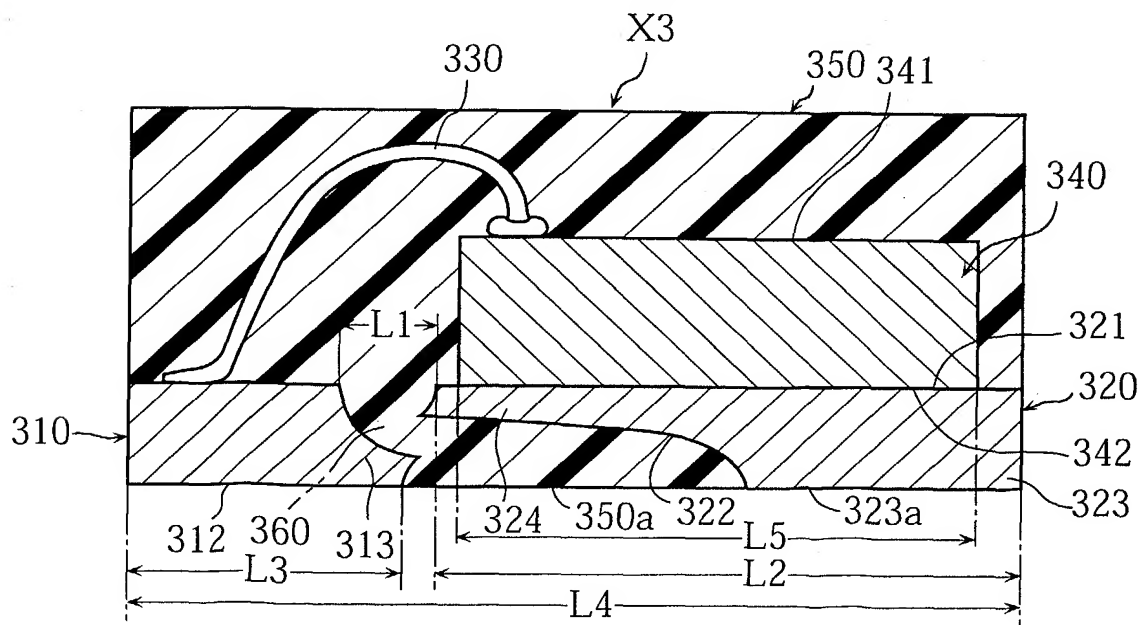


FIG. 13

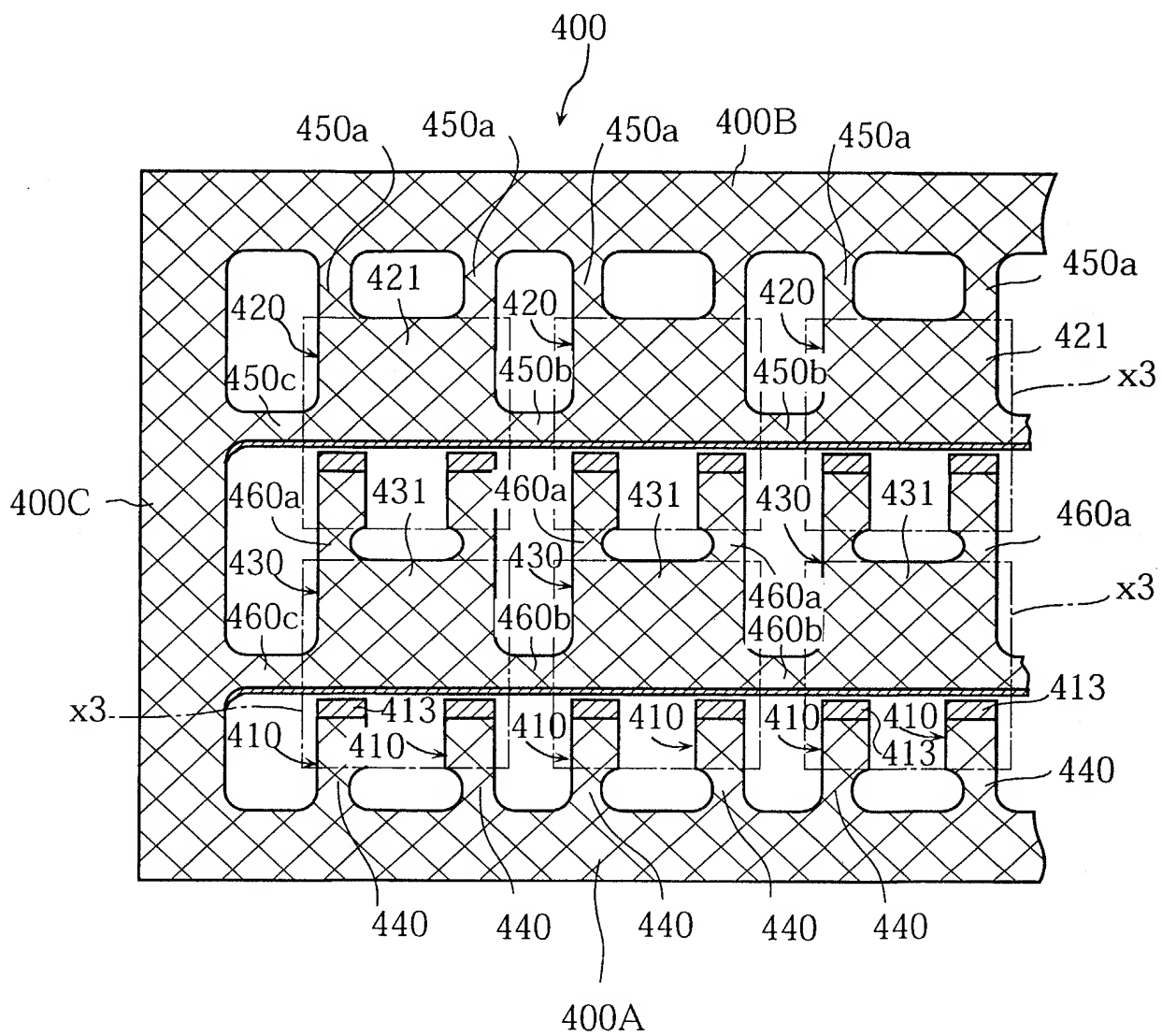


FIG. 14

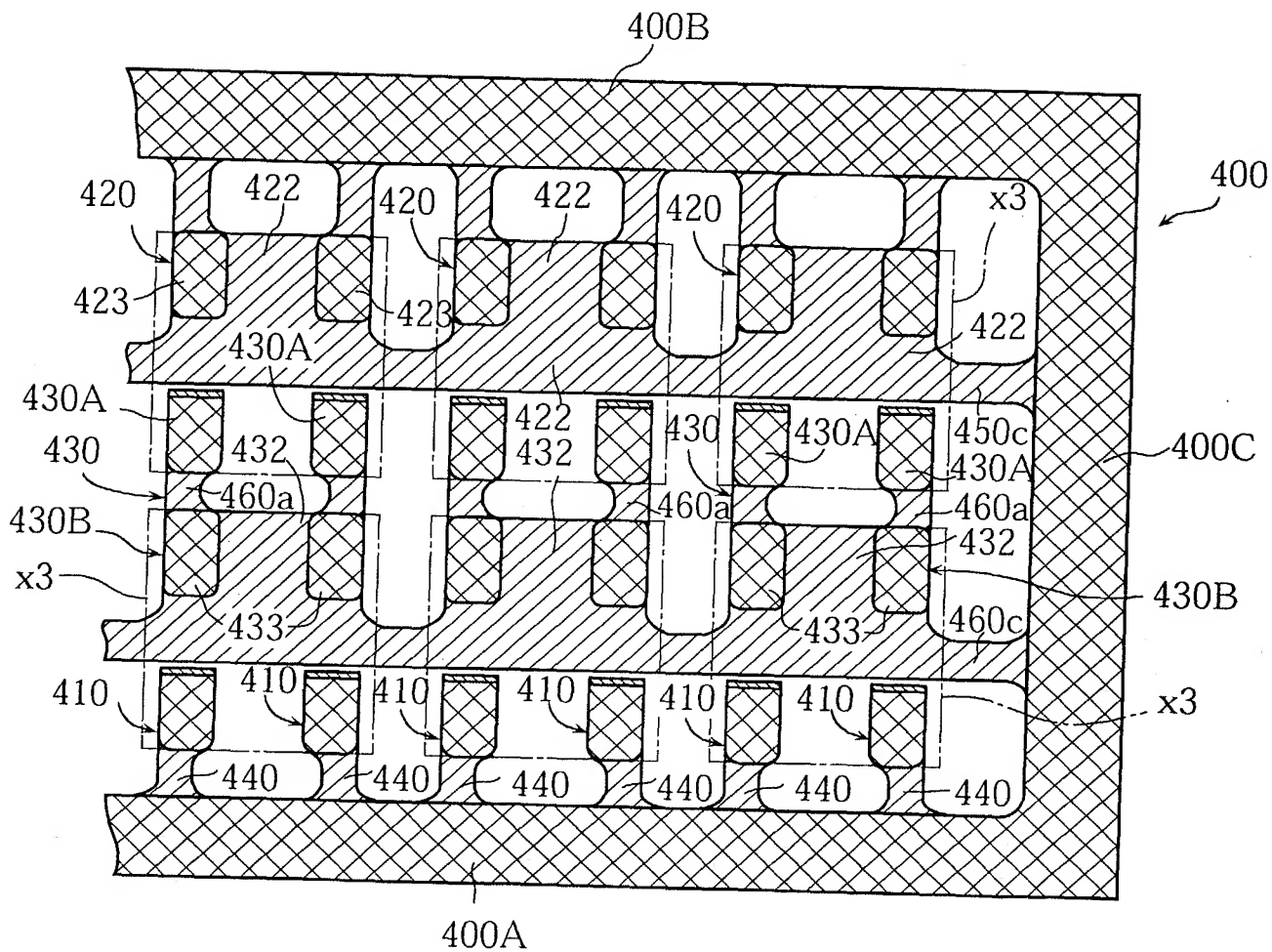


FIG. 15A

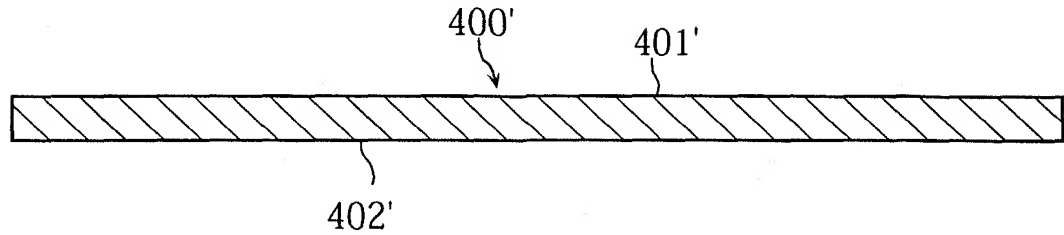


FIG. 15B

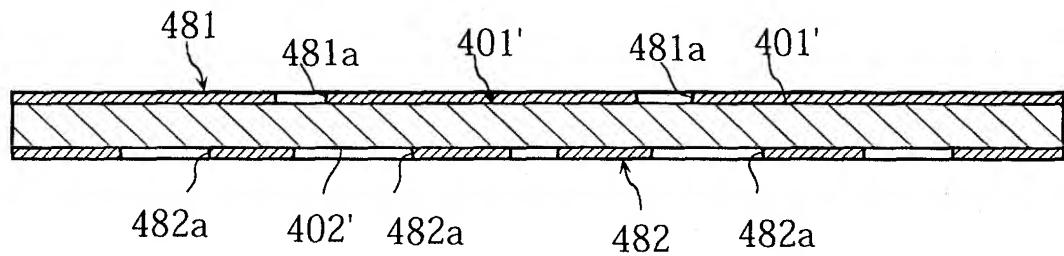


FIG. 15C

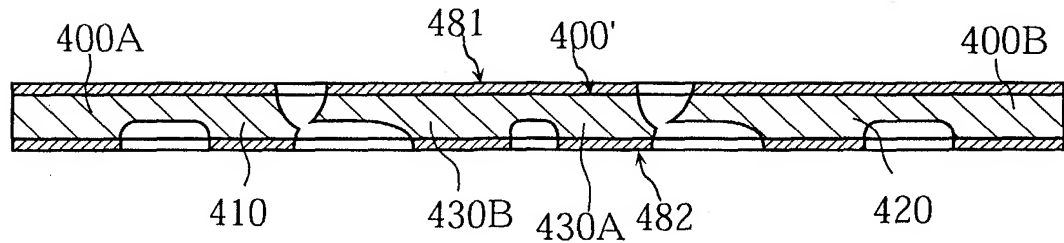


FIG. 15D

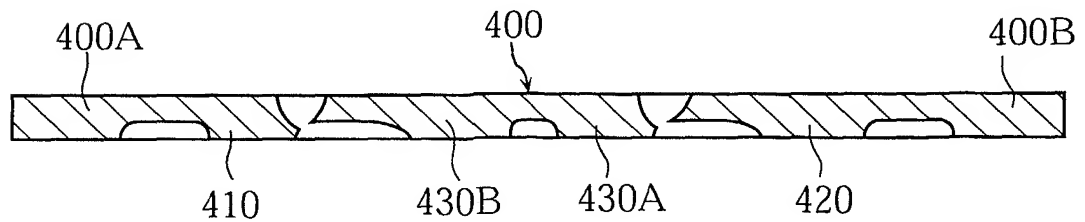


FIG. 16

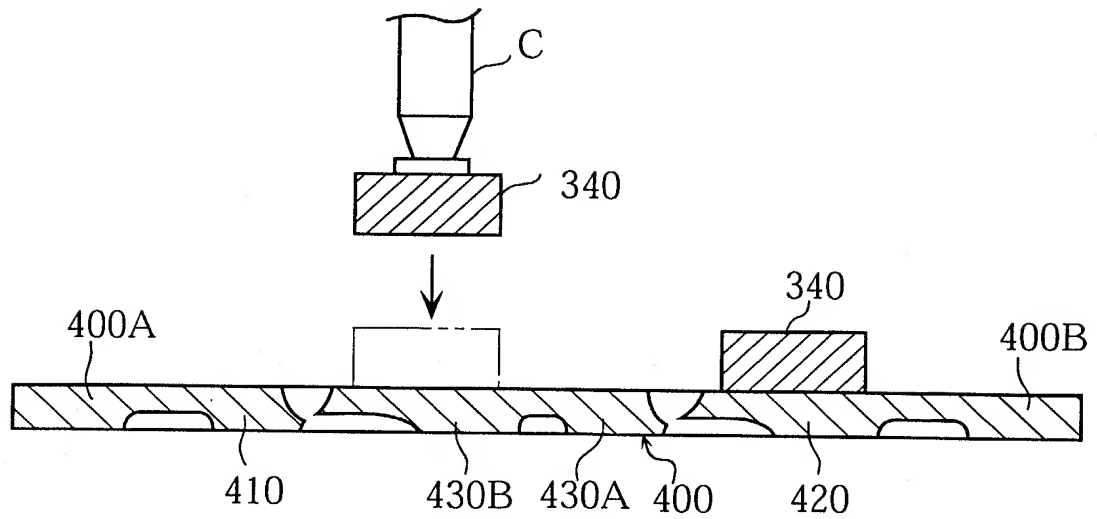


FIG. 17

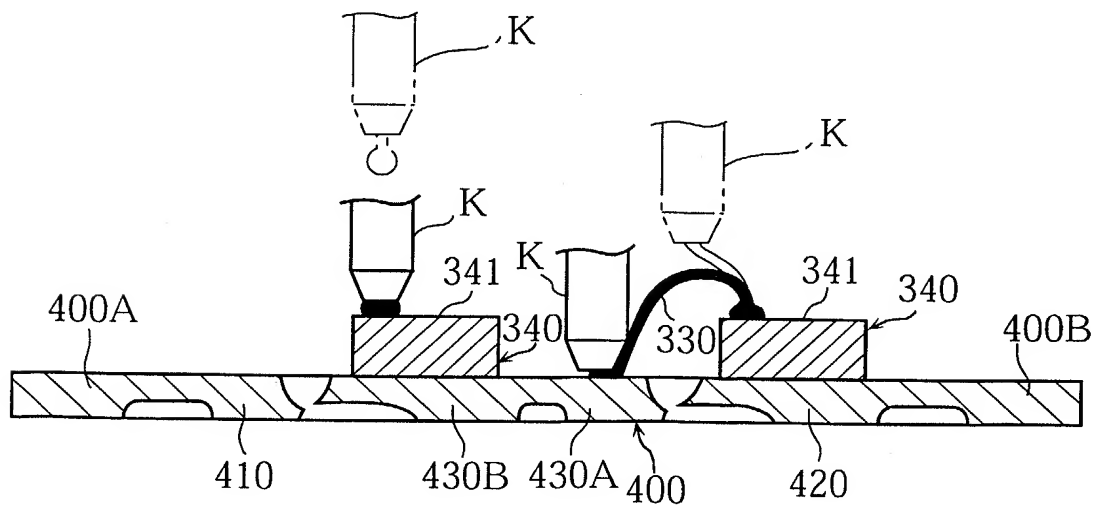


FIG. 19

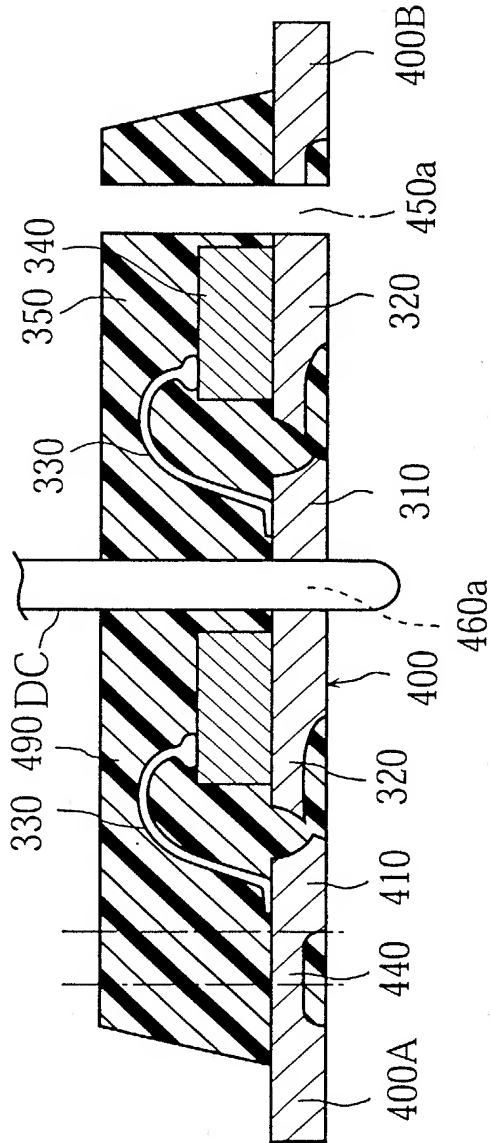


FIG. 21

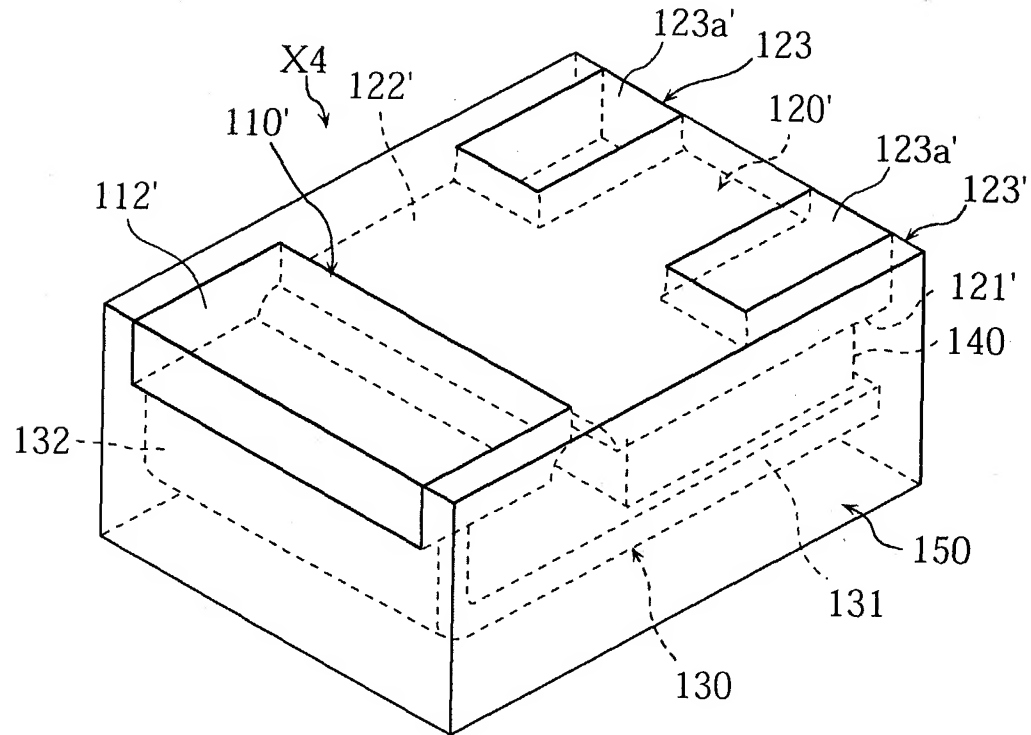


FIG. 22

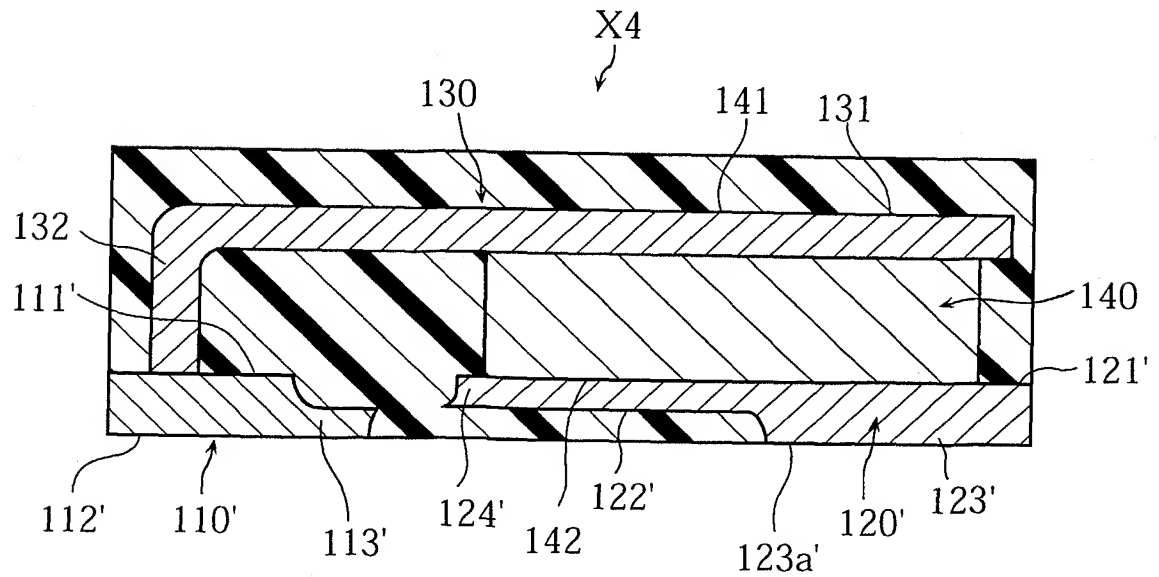


FIG. 24

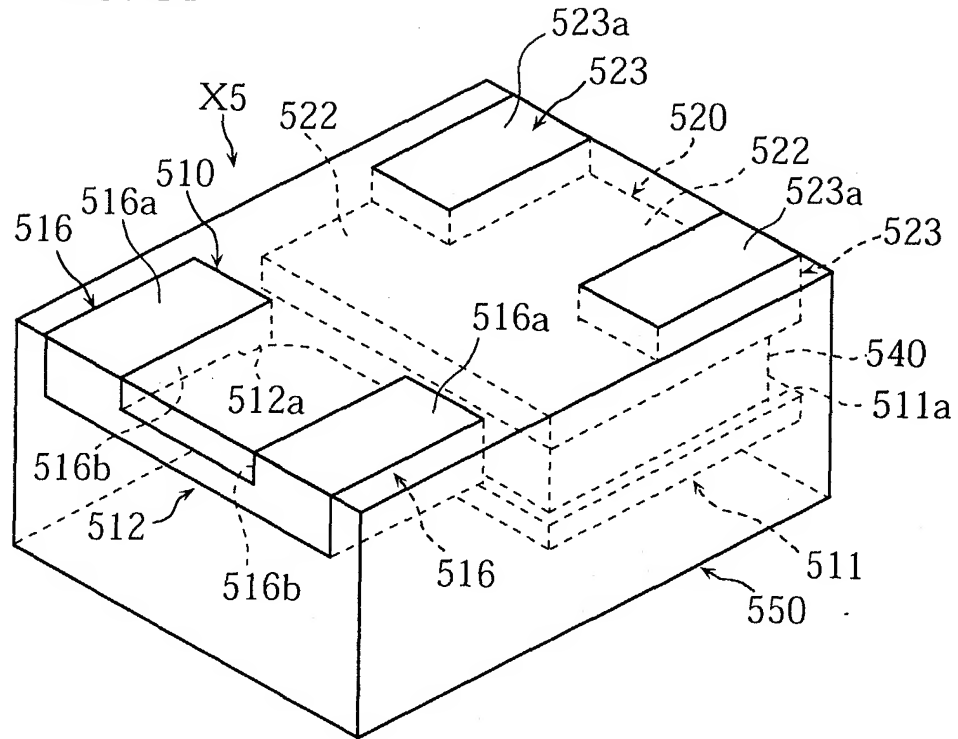
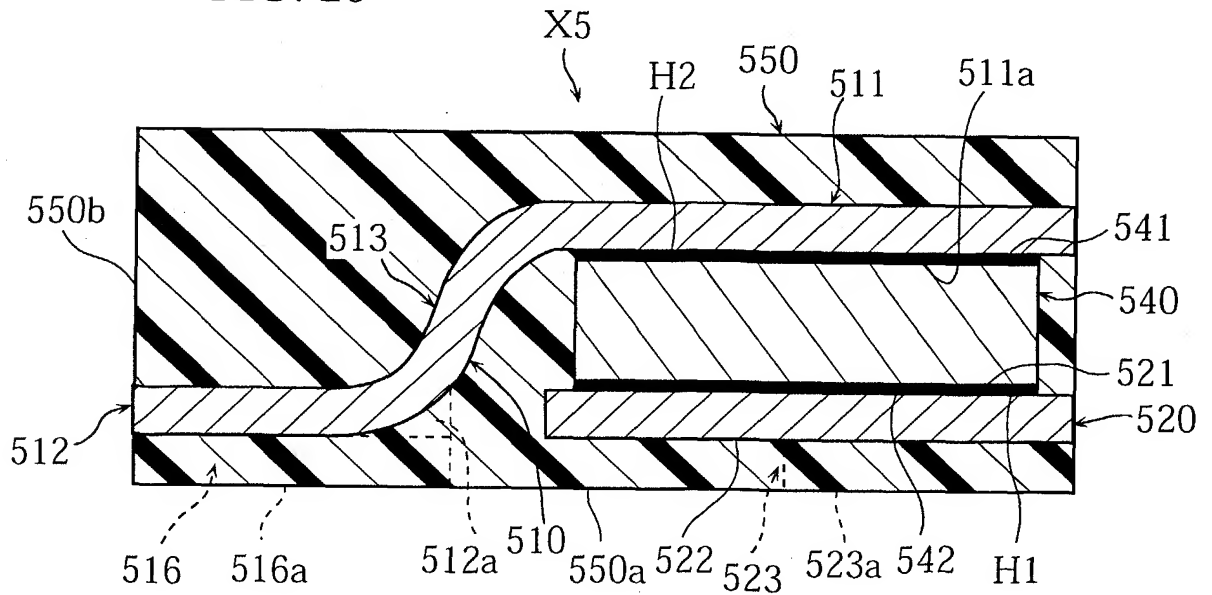


FIG. 25



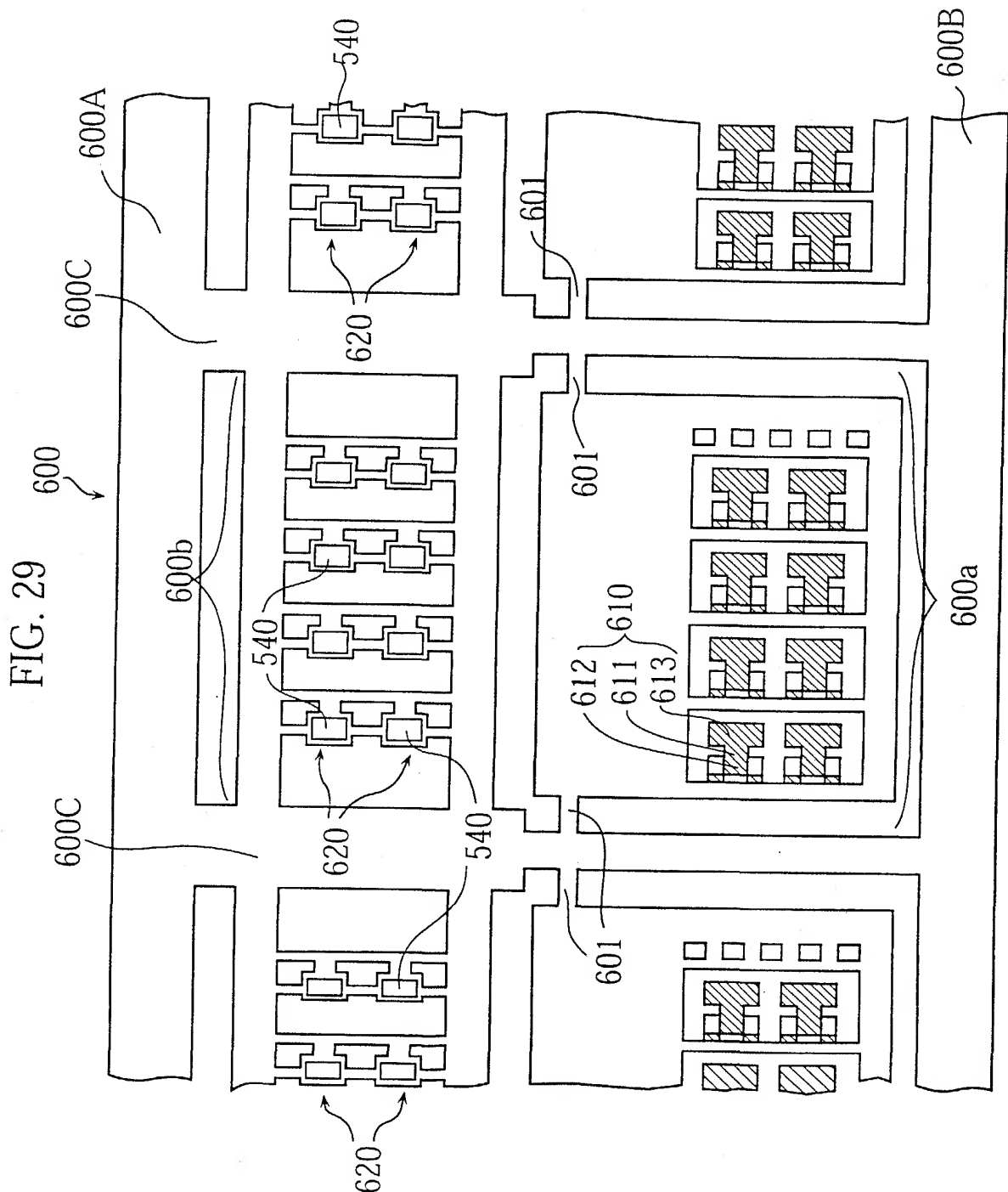


FIG. 6 is a plan view of a semiconductor device 600. The device includes a central array of elements labeled 610, 611, 612, 613, 620, and 621. A dashed line 600a separates the array from a peripheral region 601. A thick horizontal bar 600b is on the left, and a thick vertical bar 600c is at the top. A label 600B points to the left edge of the device.

FIG. 31

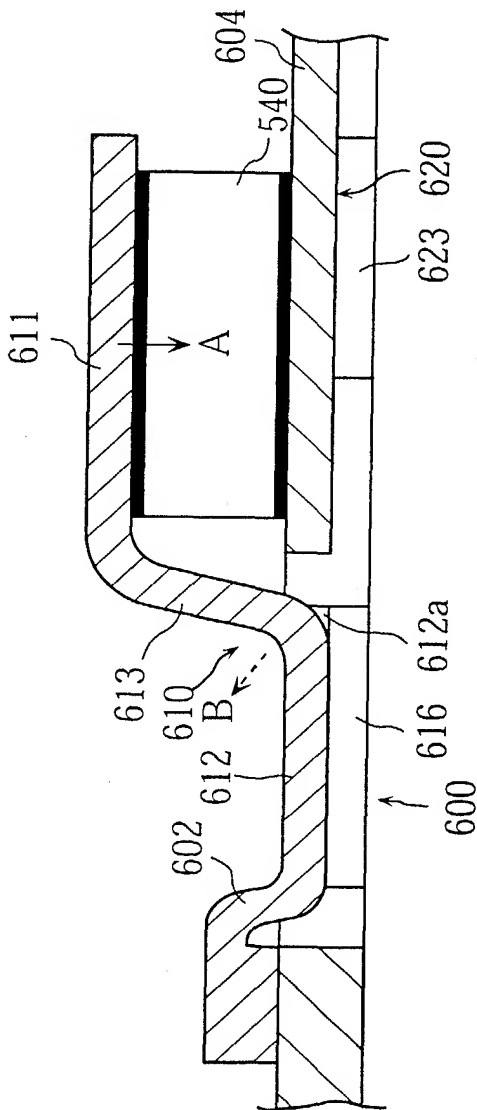


FIG. 34

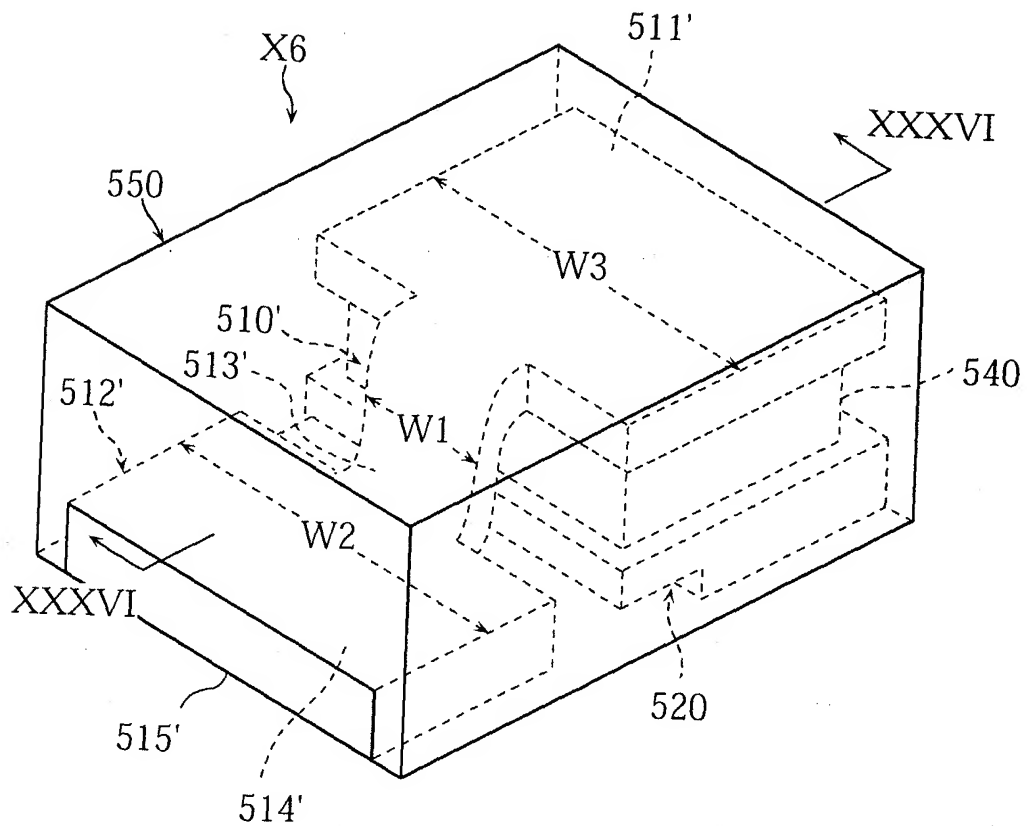


FIG. 35

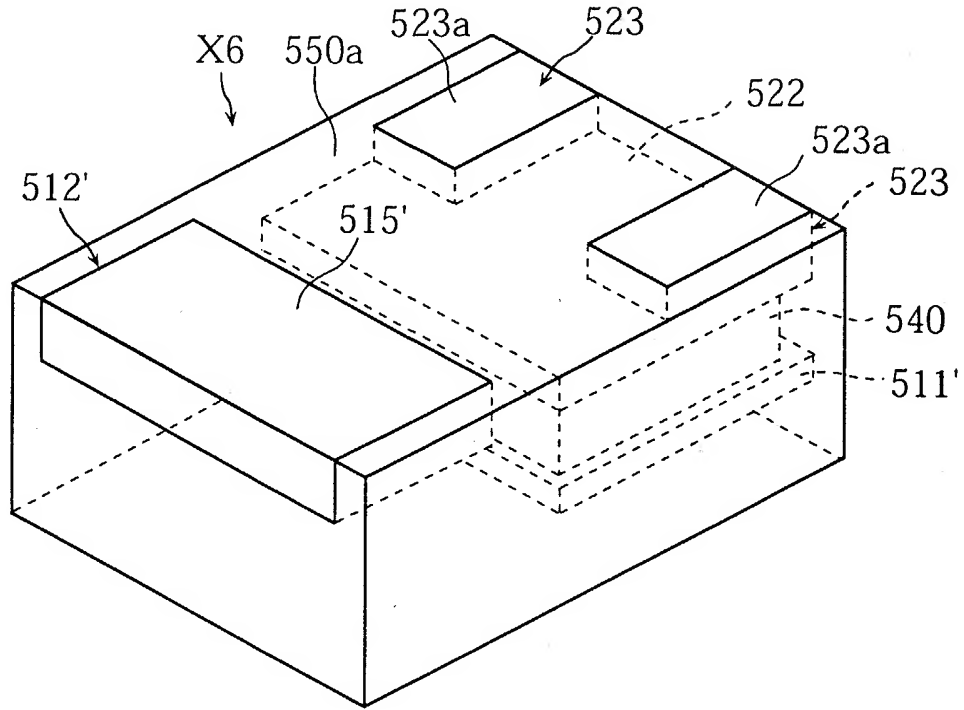


FIG. 36

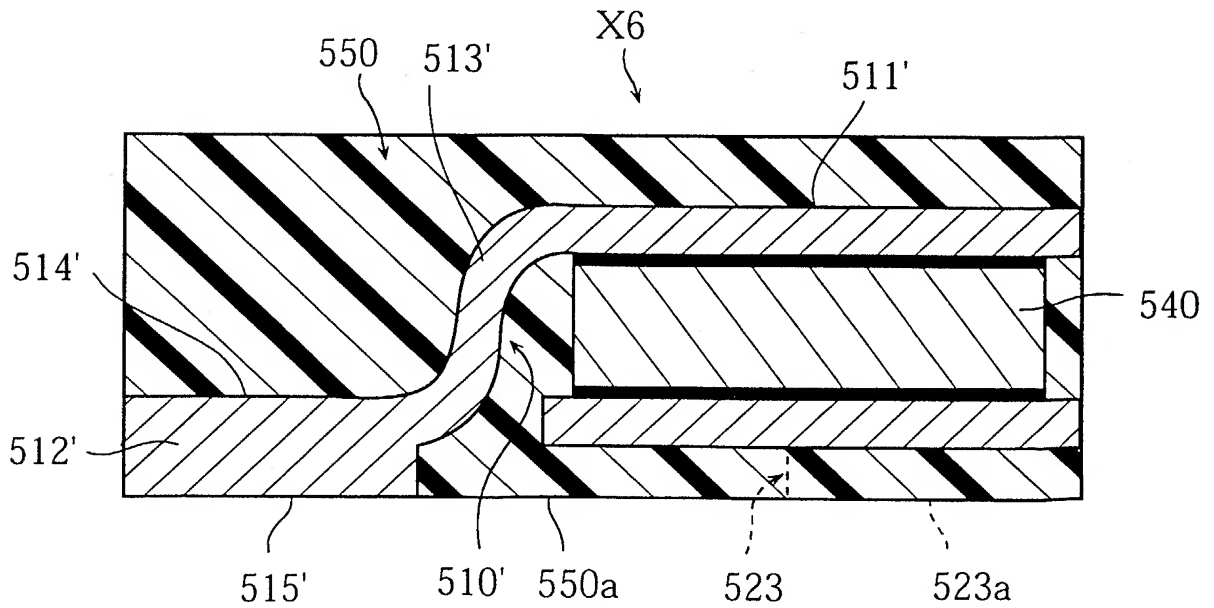


FIG. 37

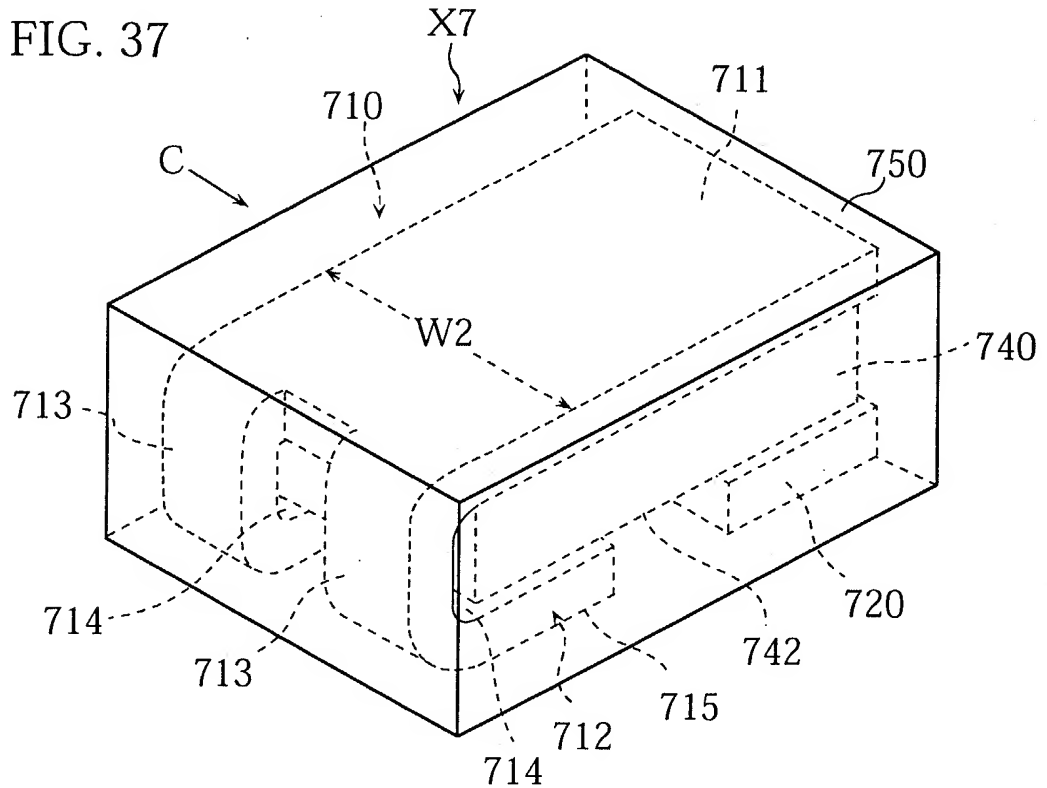
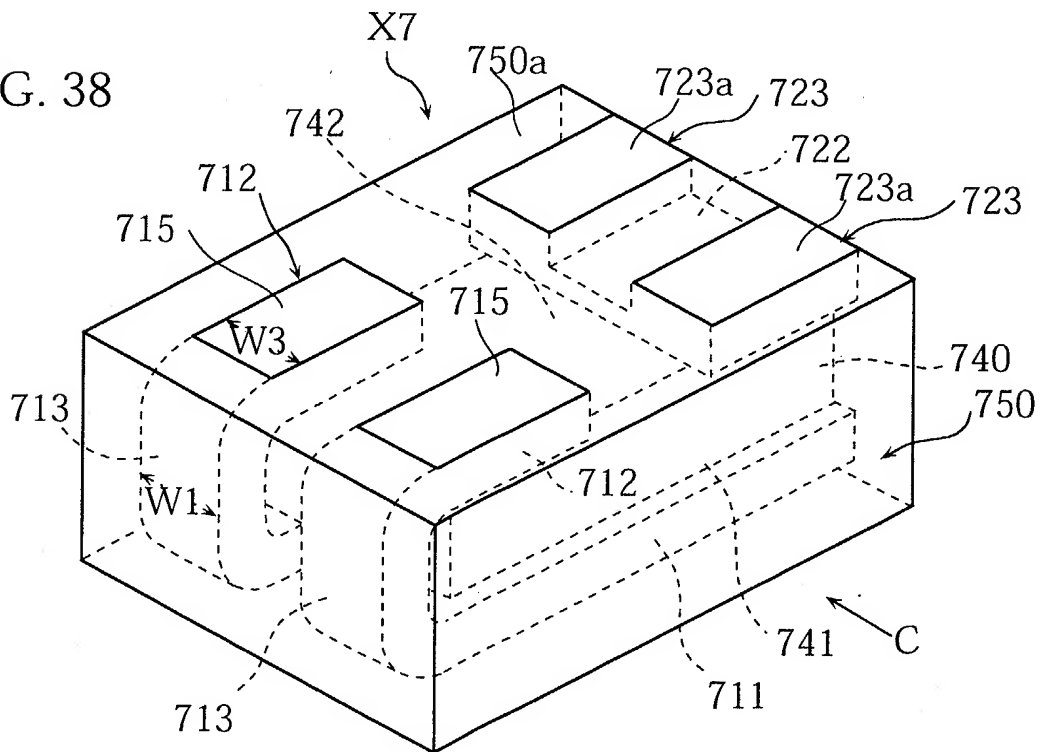


FIG. 38



[illegible]

FIG. 41

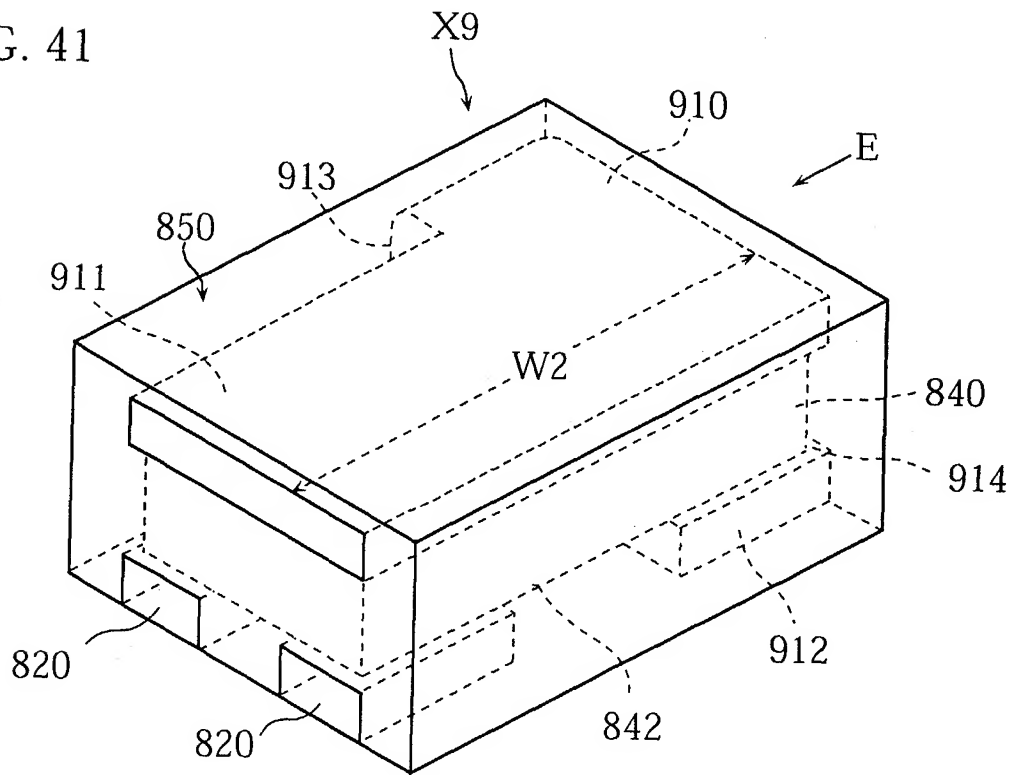


FIG. 42

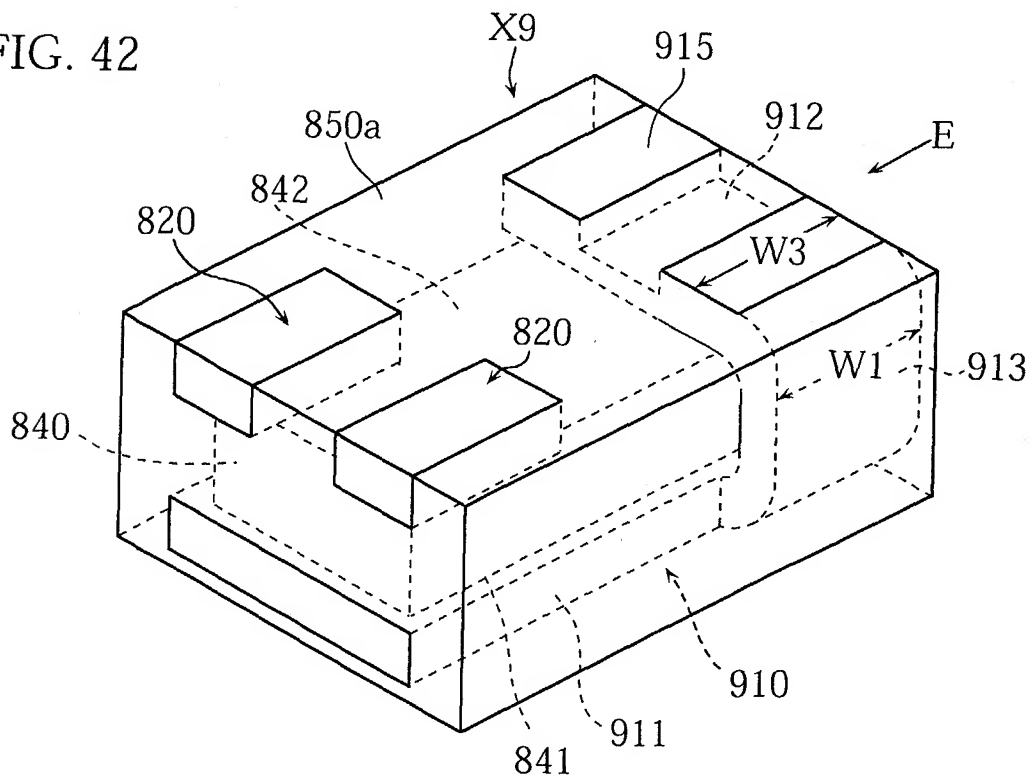


FIG. 43
PRIOR ART

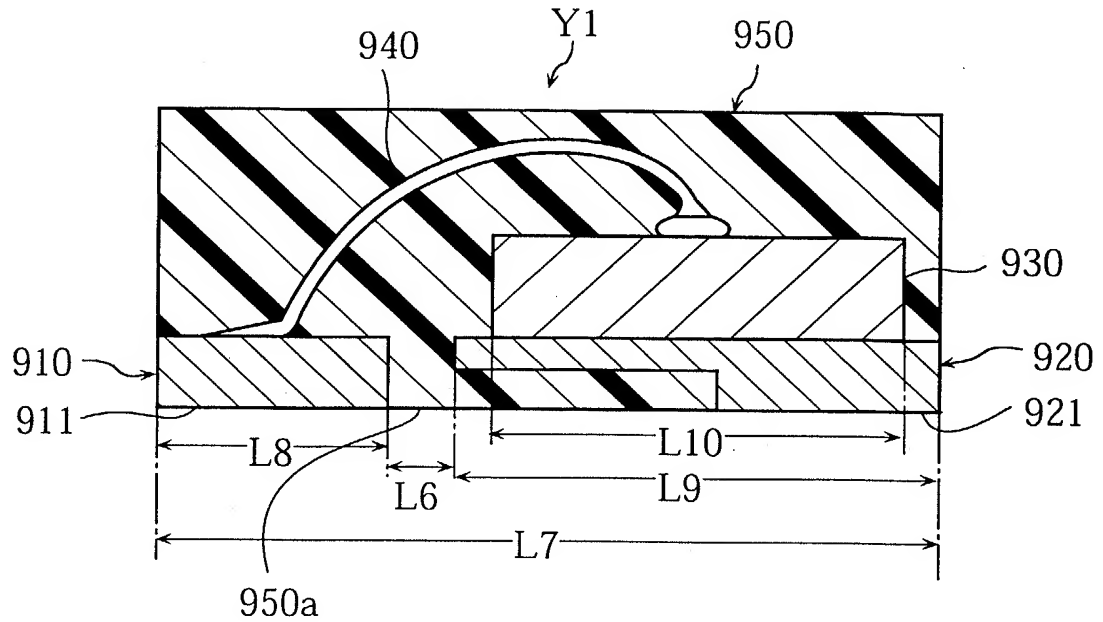


FIG. 44
PRIOR ART

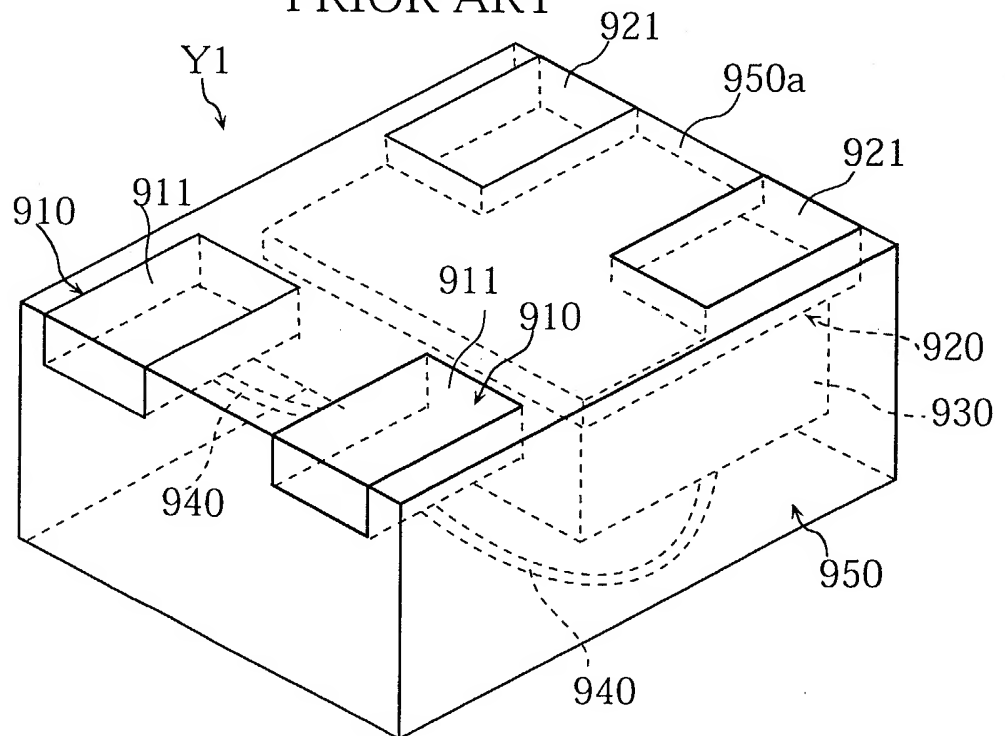


FIG. 46
PRIOR ART

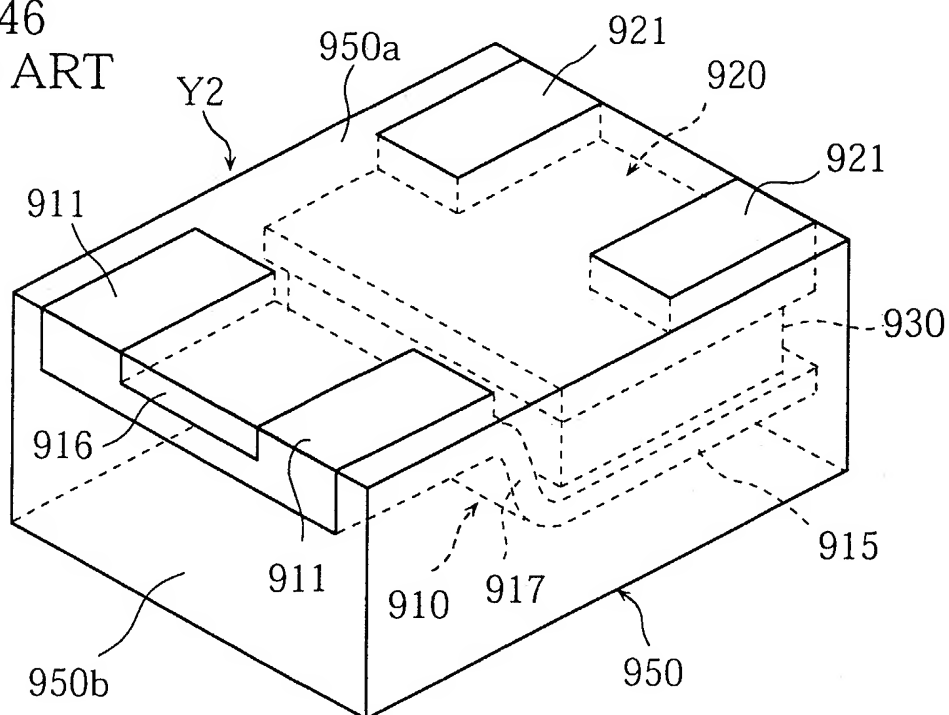


FIG. 47
PRIOR ART

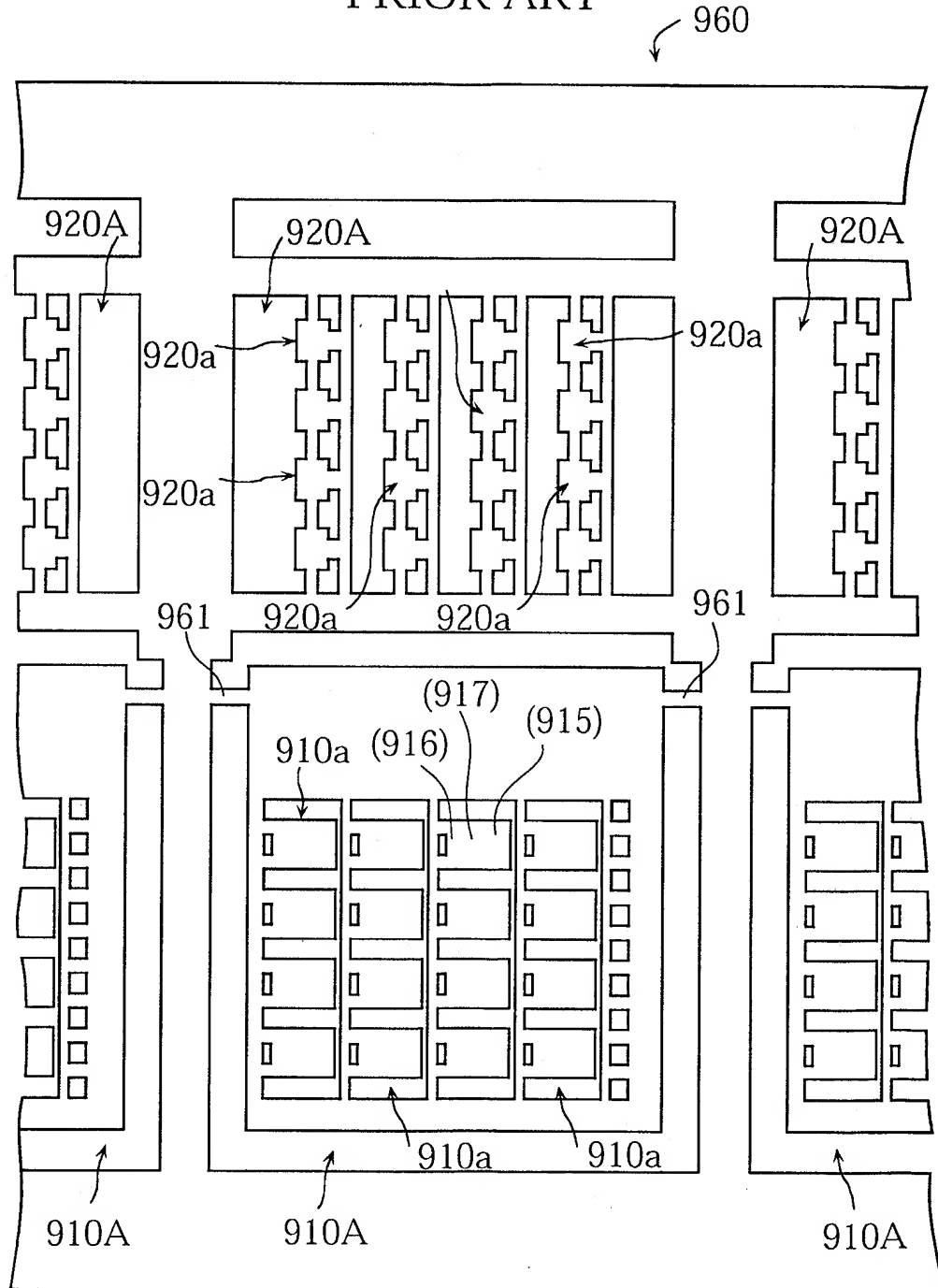


FIG. 48
PRIOR ART

